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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/985,768	11/06/2001	Kwame Osei Boateng	826.1767	4333

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EXAMINER	
SIEK, VUTHE	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	09/985,768	BOATENG, KWAME OSEI	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/06/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 09/985,768 filed on 11/6/2001. Claims 1-13 remain pending in the application.

Claim Objections

2. Claims 1 and 10-13 are objected to because of the following informalities: Phrase "redundant test stimuli", needed clarification. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5 and 7-13 are rejected under 35 U.S.C. 102(a) as being anticipated by Gui et al., "On Improving Static Test Compaction for Sequential Circuits," IEEE, Jan 3-7, 2001, pp. 111-116.

5. As to claims 1 and 10-13, Gui et al. teach compaction techniques to reduce the test sequence length (set of test stimuli) based on the reverse order restoration compaction algorithm and vector omission based compaction algorithm (redundant test stimuli elimination). During vector restoration (at least one fault is detected by one vector), once a subsequence is restored (to obtain selected essential test stimuli), the vector omission based method is applied to the restored subsequence to reduce the number of the test vector restored (to obtain a compacted set of the selected essential

(see sections 2 and 3 for detailed description). The restoration compaction algorithm and omission based compaction algorithm is described in section 2 and mixed mode compaction algorithm is described in section 3. The techniques avoid including unnecessary vectors (redundant stimuli) in a compacted set stimuli (Tp) and reduces its final length (to obtain a compacted stimuli set)

6. As to claims 2-5 and 7-9, Gui et al. teach a compacted test vector set (see mixed-mode compaction described in section 3) (as in claim 2); hierarchically repeat selection of essential test stimuli is described in section 2 and 3 (as in claim 3); optimal fault coverage (see section 2 and 3) (as in claim 4); storing information of faults in mixed mode test sequence compaction procedure (storing number of faults and point information (prefix and index fault detected) (as in claim 5); fault simulation, since a stuck-at fault and a delay fault are common practice in a fault detection simulation, the techniques as taught by Gui et al. must include a stuck-at fault model and a delay fault model (see section 3) (as in claims 7-8); performing compaction of the set of test stimuli by regarding a sequence of initializing, sensitizing and propagation subsequences as a single test stimulus (see sections2 and 3).

7. Claims 1-5 and 7-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kajihara et al., "Cost-Effective Generation of Minimal Test Sets for Stuck-at Faults in Combinational Logic Circuits," IEEE, Dec. 1995, pp. 1496-1504.

8. As to claims 1 and 10-13, Kajihara et al. teach new cost-effective heuristics for a generation of minimal test sets (compacted set of test stimuli) for a digital circuit (see whole article) comprising selecting essential test stimuli from among subsets of the set

of test stimuli, where an essential test stimulus being a test stimulus that detects at least one fault, which is detectable by no other test stimulus in one of the subsets of the test stimuli; an eliminating redundant test stimuli form among subsets of test stimuli after selecting the essential test stimuli from each subset; and an output device outputting a compacted set comprising the selected essential test stimuli (see at least section III starting page 1500, Table IV).

9. As to claims 2-5 and 7-9, Kajihara et al., teach outputting a minimum-sized subset of the set of test stimuli, which covers faults without modifying test stimuli in the minimum-sized subset, as the compacted set; hierarchically repeating selecting of essential test stimuli after eliminating of redundant test stimuli to output the compacted set comprising the selected essential test stimuli; identifying a subset of test stimuli that optimally covers a given set of faults and eliminating one or more test stimuli other than the identified test stimuli as the redundant test stimuli; storing information of faults which the set of test stimuli cover, and pointing information associating each test stimulus with the faults detectable by a corresponding test stimulus; the faults including a stuck-at fault and a delay fault; performing compaction of the set of test stimuli by regarding a sequence of initializing, sensitizing, and propagation subsequences as a single test stimulus (See at least Section III, Table IV).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being obvious over Kajihara et al., "Cost-Effective Generation of Minimal Test Sets for Stuck-at Faults in Combinational Logic Circuits," IEEE, Dec. 1995, pp. 1496-1504.

12. As to claim 6, Kajihara et al. teach using a fault simulation to search and detect essential faults of a test in the test set. As shown in Table IV, number of test of the test set, number of faults and number of check are described. It is well known to practitioners in the art that a counter is used to store information related application in order to facilitate the process. Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to have stored counter information as recited in the claim in order to facilitate the fault simulation to obtain information as shown in Table IV as expected, thereby a compacted set comprising of essential test stimuli is finally obtained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER